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INSTRUCTION INFORMATION FOR THE G-8815 PROGRAMMABLE FS TRANSMITTER

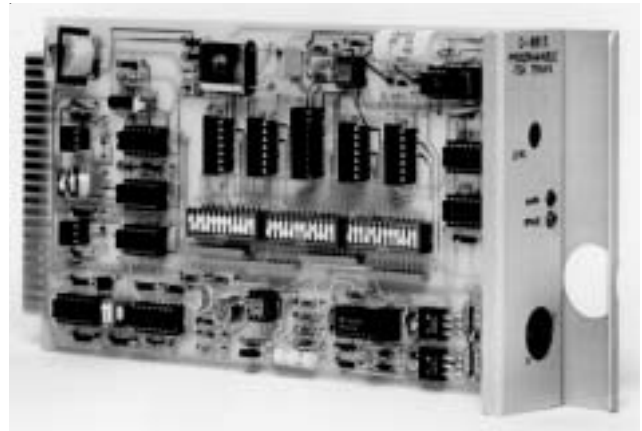
GENERAL DESCRIPTION

The G-8815 is a single card, frequency shift transmitter capable of having the mark, center and space frequencies for each frequency programmed by a block of 12 switches. The G-8815 is intended as a universal spare for the G-8080 section A and for most configurations of the G-7605 FS transmitters. In using the G-8815, one should be aware of the across-the-band loading of the output stage. Adjacent channels will be loaded by the 3000 ohm output impedance of the G-8815; therefore, the signal levels of the adjacent channels may have to be adjusted by up to 10%, depending on the number of channels involved.

Along with the on-card programming switches for mark, center and space, switches are provided to program 2F/3F operation, enable or disable sampling, select sampling rates of 15, 30, or 60 Hz and to select voltage or current loop keying.

THEORY OF OPERATION

Referring to the schematic of the G-8815, U16 provides the driver stage to drive tones onto the transmission line. T1 isolates the tone equipment from the media and



drives through the 2700 ohm resistor, R35, to exhibit the 3000 ohm across-the-spectrum impedance. The second stage of U16 and the Q4, and Q5 driver form an output amplifier with a gain of 5. Q1, when turned on, shunts the input to the driver stage to ground to squelch the output. The level at TP4 should be approximately 1.5 volts peak-to-peak to common with R26 turned up completely. R25 and C8 serve to filter the sampling steps of the switch-capacitor filter output to reconstruct a smooth, continuous wave form.

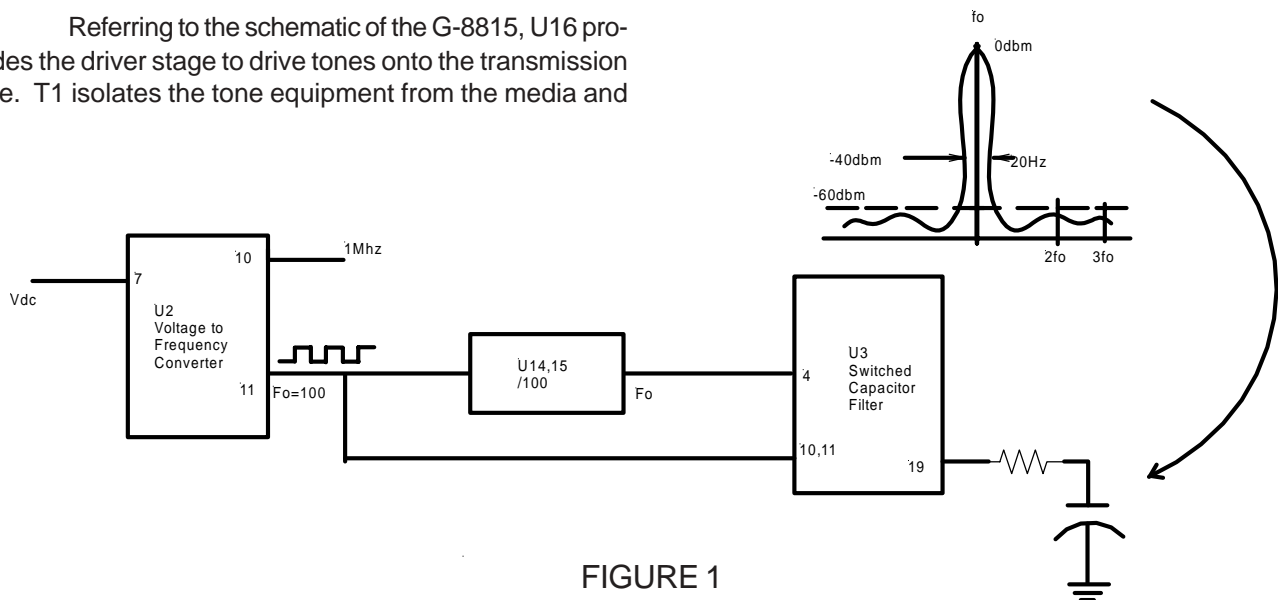


FIGURE 1

Referring to Figure 1, U2 is a voltage-to-frequency converter which generates an output at pin 11 that is the ratio between the clock frequency at TP3 and the dc level of the input voltage at pin 7 of U2. The switched-capacitor filter network, U3, is configured as a high-Q bandpass filter to remove harmonics from its input square wave. For optimum performance, the clock frequency at pins 10 and 11 is set to 100 times the center frequency of the bandpass filter function. This combination of U2, U3, U14 and U15 shown in Figure 1 creates a sine wave output that is adjustable by an analog voltage. The $F_o \times 100$ square wave from the voltage-to-frequency converter is used directly to clock the switch-capacitor filter. The $F_o \times 100$ square wave is at the fundamental frequency of interest. The bandpass characteristics of the switch-capacitor filter attenuate all harmonics better than 55 db to produce a very clean output. Due to the function of the voltage-to-frequency converter, as the voltage in is varied over a range the output F_o is a pure sine wave of proportion.

U1 is a 12-bit digital-to-analog converter which allows the user to set the frequency desired digitally with switch settings and produce a dc level in the range of the input to the voltage-to-frequency converter. Trimmer R4, the calibration set point adjustment, is aligned properly when the output frequency is 3500 Hz and all switches are closed on the bank of switches to

which the unit is keyed. Generally, do not key either mark or space; close all switches on the center switch bank and tune R4 for 3500 Hz. U1 and U4 are essentially a digitally programmed gain amplifier with a reference input of approximately 6.2 Vdc from the 1N823A zener diode, CR10. U5 through U8 'OR' the mark, center and space switch banks onto the 12-bit address lines of the digital-to-analog converter. The logic controlled by the input keying circuitry selects the bank of switches needed to key the frequency; i.e. when the G-8815 is keyed to mark, the mark bank of switches will be driven high on their common side. If a switch is open or its bank is not keyed high, that input to the OR-gate will be low, therefore not affecting the code presented to the digital-to-analog converter.

U9 and U10 provide a frequency to the select logic to perform the sampling operation when enabled, U9 serves as the first divider stage dividing the clock by either 16,384 or 8,192 to yield 61 Hz or 122 Hz, respectively. The next stage, U10, allows selection of either divide-by-2 or divide-by-4 to produce the frequencies specified in the sampling frequency table shown on the schematic. S6 allows the user either to drive the U10 divider into reset, thereby disabling the sampler circuit, or to enable the sampler control from the keying logic. This control of the reset by the logic allows sampling pulses only when both mark and space are keyed.

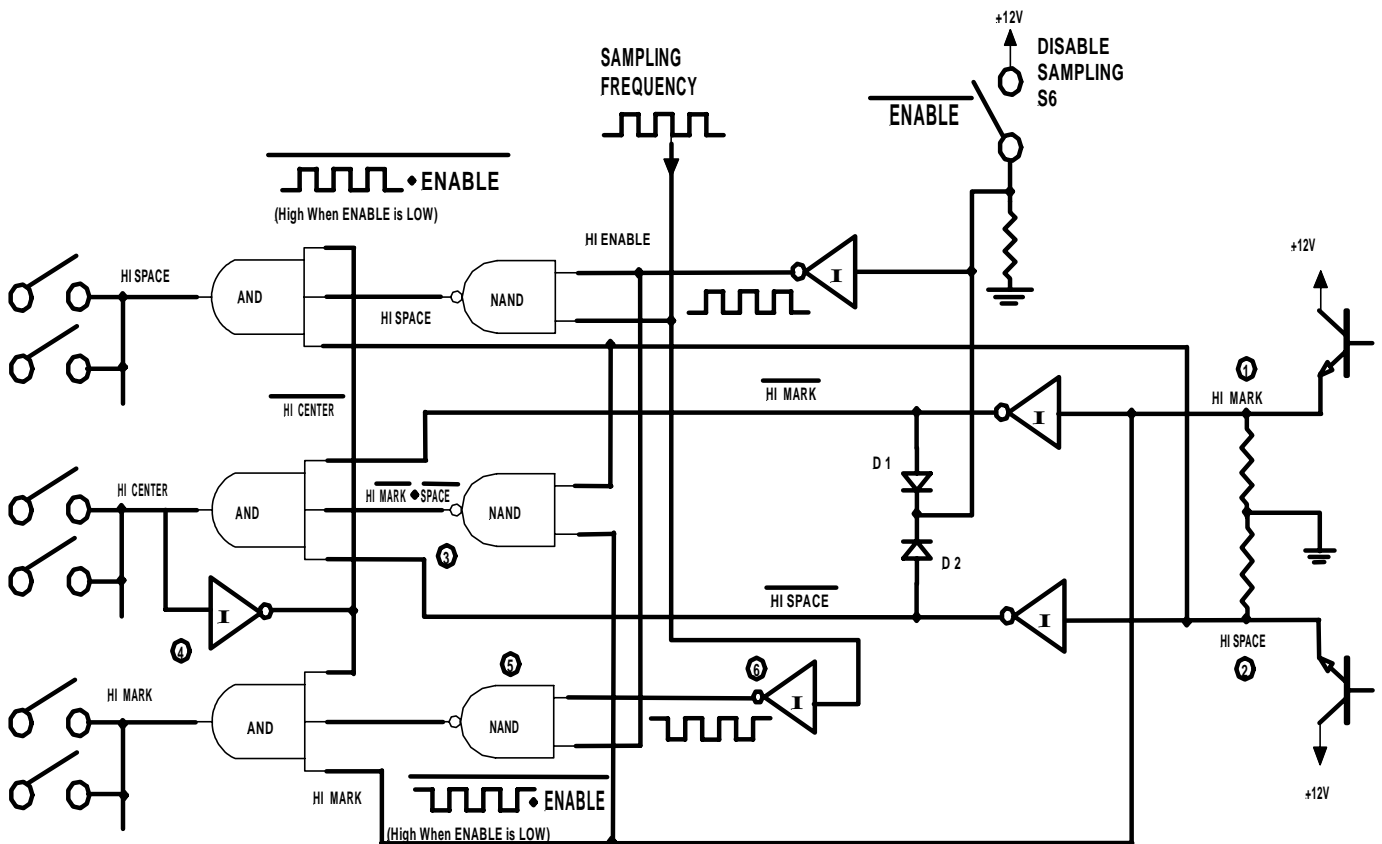


FIGURE 2

The input stage allows either the use of CMOS (0, 12 Vdc) dyeing into the logic circuitry by closing S5a and S5b or, by opening S5a and S5b, the CMOS coupling to the inputs is broken and the opto couplers U17 and U18 are used for current loop keying. These opto couplers serve two purposes; to isolate the keying circuit from the G-8815 CMOS logic input and to improve noise immunity by the minimum loop current required. Additional noise immunity is realized when the signal level is greater than 12 volts by switching C1 and C2 to their '1' and '2' positions, thereby placing a 6.3 volt threshold on the keying voltage.

The keying logic illustrated in Figure 2 depicts the signal logic of the different stages within. The bank of switches for center frequency is selected when both the mark and space isolators are not keyed and, therefore, points 1 and 2 are at 0 volts. The NAND gate at point 3 disables the center output if either mark or space is keyed. When both are not keyed the NAND gate's output enables the center frequency output AND gate.

When the center frequency criteria is satisfied, the inverter at point 4 insures that the mark and space outputs are driven low. With or without sampling enabled, when the mark or space input is keyed, the center frequency output is disabled immediately, which in turn enables the mark or space outputs. When mark is keyed, the only line that is not yet determined to be high at the input to the mark AND is that input coming from the NAND at point 5. When sampling is disabled either by S6 or because both mark and space are not keyed driving +12 V through D1 and/or D2, the enable line into the NAND will be low causing the output of the NAND at point 5 to be driven high.

By this action the mark bank of switches is then selected. The same logic flow occurs for the space output AND. When both mark and space are keyed, the enable line will go low since S6 is open (to enable sampling) and since the anodes of D1 and D2 are now both low. The enable line at the input of the NAND at point 5 will be driven high to enable the pulses from the sampler output to the AND outputs. Since all other lines are high at the inputs to the output ANDs, whenever the sampling pulses go high at the AND, that bank of switches will be selected. The inverter at point 6 inverts the pulse train with respect to that seen at the space AND, thereby assuring that mark and space will be keyed alternately.

FREQUENCY SELECTION

With R4 adjusted for 3500 Hz with all switches closed, the resolution of frequency is approximately 0.85 Hz. Each frequency should be able to be programmed to within 1 Hz of the desired value. Table 1 lists the approximate contribution of each switch position to the output frequency.

SWITCH POS.	FREQ.	SWITCH POS.	FREQ.
12	1752	6	27
11	878	5	14
10	441	4	7
9	222	3	3
8	109	2	1.3
7	55	1	0.85

TABLE 1

The best method of programming the frequencies to that desired is to key the G-8815 to mark, center or space and then encode the frequency while monitoring the output with a frequency counter. For example, say the frequency of interest is F_0 . Close S12 and if the measured frequency F_r is less than F_0 , close S11. If, when S12 is closed, $F_r > F_0$, open S12 and then close S11. If $F_r < F_0$, close S10; if $F_r > F_0$, open S11 and close S10. Continue the process until F_r is at least within 1 Hz of the desired frequency. This algorithm for frequency programming is illustrated in Figure 3.

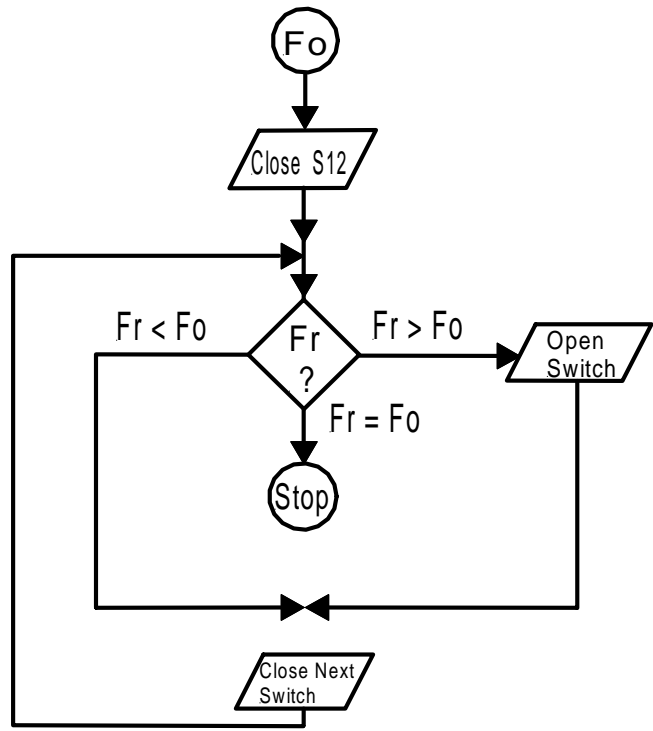


FIGURE 3

Table 2 shows some examples of typical switch settings encountered for frequency programming.

CENTER FREQUENCY	BANDWIDTH	Mark Sw. Setting	Center Sw. Setting	Space Sw. Setting
1275 Hz	50 Hz	1,2,5,6,7,8,9,11	2,3,5,7,8,9,11	1,4,5,6,8,9,11
2520 Hz	240 Hz	3,4,5,11,12	2,3,4,8,9,10,12	9,10,12
1860 Hz	480 Hz	1,6,8,9,12	1,2,3,8,12	1,3,4,6,7,9,10,11

TABLE 2

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